2N7000

Siliconix

N-Channel Enhancement Mode
MOSPOWER FETlington™

APPLICATIONS

- CMOS or TTL Logic Compatible
- Bipolar Darlington Replacement
- Lamp, Relay Driver or Buffer
- Analog Signal Switching

PRODUCT SUMMARY

Part Number	BV_{DSS} Volts	$r_{DS(ON)}$ (ohms)	Package
2N7000	60	5	TO–92

PIN 1 – Source
PIN 2 – Gate
PIN 3 – Drain



TO–92

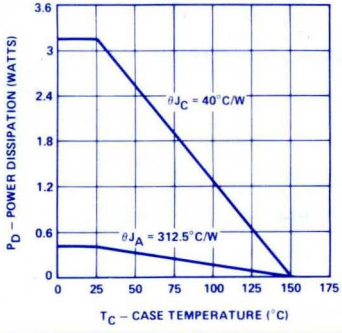
NEW
LOGIC-TO-LOAD
DESIGN
5 Volts in-100 mA out

ABSOLUTE MAXIMUM RATINGS (T_C = 25° C unless otherwise noted)

	Parameter	2N7000	Units
V_{DS}	Drain-Source Voltage	60	V
V_{DGR}	Drain-Gate Voltage (R_{GS} = 1 MΩ)	60	V
I_D @ T_C = 25° C	Continuous Drain Current	±200	mA
I_D @ T_C = 100° C	Continuous Drain Current	±123	mA
I_{DM}	Pulsed Drain Current[1]	±500	mA
V_{GS}	Gate-Source Voltage	±40	V
P_D	Max. Continuous Power Dissipation	400	mW
P_D	Max. Pulsed Power Dissipation[2]	3.125	W
Junction to Case	Linear Derating Factor	25	mW/° C
Junction to Ambient	Linear Derating Factor	3.2	mW/° C
T_J Tstg	Operating and Storage Temperature Range	−55 To +150	° C
Lead Temperature	(1/16" from case for 10 secs.)	300	° C

1 **Pulse Test:** Pulsewidth ≤ 300μsec, Duty Cycle ≤ 2%
2 One Second Single, Power Pulse

Power Derating



ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

STATIC

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	2N7000	60	80		V	V_{GS} = 0 I_D = 10 μA
$V_{GS(th)}$	Gate-Threshold Voltage	2N7000	0.8	1.8	3	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate-Body Leakage Forward	2N7000		1	10	nA	V_{GS} = +15V
I_{GSSR}	Gate-Body Leakage Reverse	2N7000		−1	−10	nA	V_{GS} = −15V
I_{DSS}	Zero Gate Voltage Drain Current	2N7000		0.1	1	μA	V_{DS} = 48V , V_{GS} = 0
		2N7000		0.1	1	mA	V_{DS} = 48V , V_{GS} = 0 T_C = 125°C
$I_{D(on)}$	On-State Drain Current[1]	2N7000	75	100		mA	V_{GS} = 4.5V , V_{DS} = 10V
$V_{DS(on)}$	Static Drain-Source On-State Voltage[1]	2N7000		1.2	2.5	V	V_{GS} = 10V , I_D = 0.5A
		2N7000			0.40	V	V_{GS} = 4.5V , I_D = 75 mA
$R_{DS(on)}$	Static Drain-Source On-State Resistance[1]	2N7000		2.4	5	Ω	V_{GS} = 10V , I_D = 0.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance[1]	2N7000		4.3	9	Ω	V_{GS} = 10V, I_D = 0.5A, T_C = 125°C

DYNAMIC

g_{fs}	Forward Transductance[1]	2N7000	100	200		mS(℧)	V_{DS} = 10V, I_D = 0.2A
C_{iss}	Input Capacitance	2N7000		30	60	pF	V_{GS} = 0 , V_{DS} = 25V f = 1 MHz
C_{oss}	Output Capacitance	2N7000		14	25	pF	
C_{rss}	Reverse Transfer Capacitance	2N7000		2	5	pF	
$t_{(ON)}$	Turn-On Time	2N7000		6	10	ns	V_{DD} = 15V , I_D ≅ 0.50A R_g = 25Ω , R_L = 25Ω
$t_{(OFF)}$	Turn-Off Time	2N7000		6	10	ns	(MOSFET switching times are essentially independent of operating temperature.)

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	2N7000		33	40	°C/W	
R_{thJA}	Junction-to-Ambient	2N7000			312.5	°C/W	Free Air Operation

BODY-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	2N7000			−0.2	A	Modified MOSPOWER symbol showing the integral P N Junction rectifier
I_{SM}	Source Current[1] (Body Diode)	2N7000			−0.5	A	
V_{SD}	Diode Forward Voltage[1]	2N7000		−0.85		V	T_C=25°C, I_S=−0.2A, V_{GS} = 0

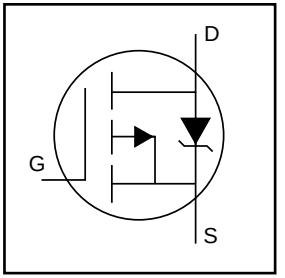
1 Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

International
IOR Rectifier

IRF9Z24N

HEXFET® Power MOSFET

- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- P-Channel
- Fully Avalanche Rated



V_{DSS} = -55V

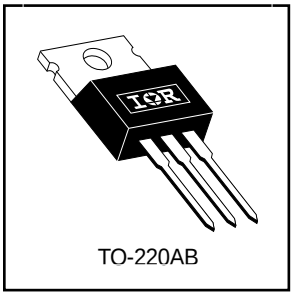
$R_{DS(on)}$ = 0.175Ω

I_D = -12A

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



TO-220AB

Absolute Maximum Ratings

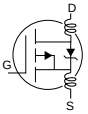
	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ -10V	-12	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ -10V	-8.5	
I_{DM}	Pulsed Drain Current ①	-48	
P_D @T_C = 25°C	Power Dissipation	45	W
	Linear Derating Factor	0.30	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	96	mJ
I_{AR}	Avalanche Current①	-7.2	A
E_{AR}	Repetitive Avalanche Energy①	4.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	3.3	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient	——	62	

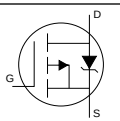
Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-55	——	——	V	V_{GS} = 0V, I_D = -250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	-0.05	——	V/°C	Reference to 25°C, I_D = -1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	0.175	Ω	V_{GS} = -10V, I_D = -7.2A ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	——	-4.0	V	V_{DS} = V_{GS}, I_D = -250µA
g_{fs}	Forward Transconductance	2.5	——	——	S	V_{DS} = -25V, I_D = -7.2A
I_{DSS}	Drain-to-Source Leakage Current	——	——	-25	µA	V_{DS} = -55V, V_{GS} = 0V
		——	——	-250		V_{DS} = -44V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V
Q_g	Total Gate Charge	——	——	19	nC	I_D = -7.2A
Q_{gs}	Gate-to-Source Charge	——	——	5.1		V_{DS} = -44V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	——	10		V_{GS} = -10V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	——	13	——	ns	V_{DD} = -28V
t_r	Rise Time	——	55	——		I_D = -7.2A
$t_{d(off)}$	Turn-Off Delay Time	——	23	——		R_G = 24Ω
t_f	Fall Time	——	37	——		R_D = 3.7Ω, See Fig. 10 ④
L_D	Internal Drain Inductance	——	4.5	——	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	——	7.5	——		
C_{iss}	Input Capacitance	——	350	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	170	——		V_{DS} = -25V
C_{rss}	Reverse Transfer Capacitance	——	92	——		f = 1.0MHz, See Fig. 5



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	-12	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	-48		
V_{SD}	Diode Forward Voltage	——	——	-1.6	V	T_J = 25°C, I_S = -7.2A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	47	71	ns	T_J = 25°C, I_F = -7.2A
Q_{rr}	Reverse RecoveryCharge	——	84	130	µC	di/dt = -100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				



Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 3.7mH R_G = 25Ω, I_{AS} = -7.2A. (See Figure 12)

③ I_{SD} ≤ -7.2A, di/dt ≤ -280A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

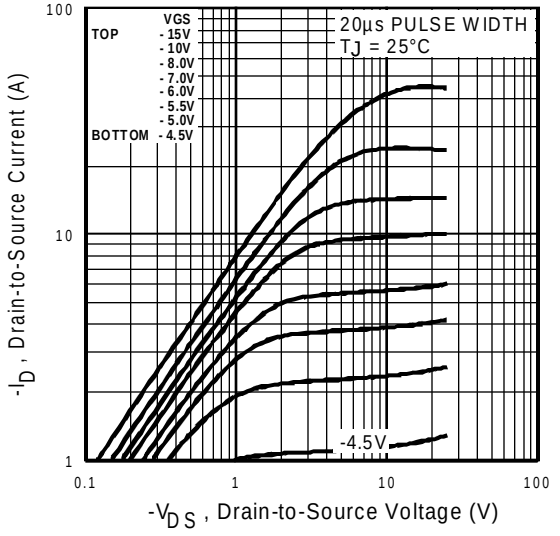


Fig 1. Typical Output Characteristics,

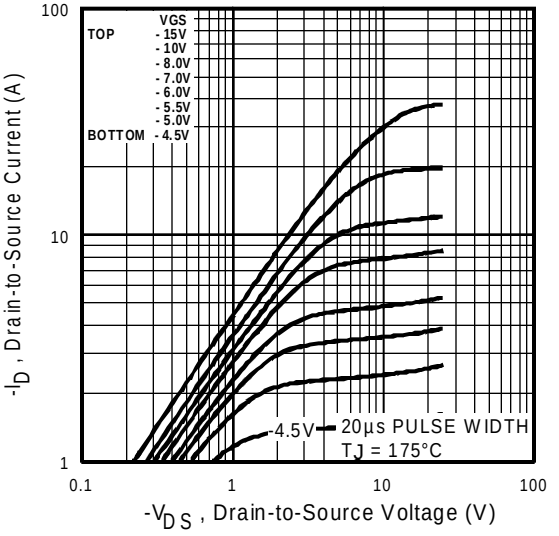


Fig 2. Typical Output Characteristics,

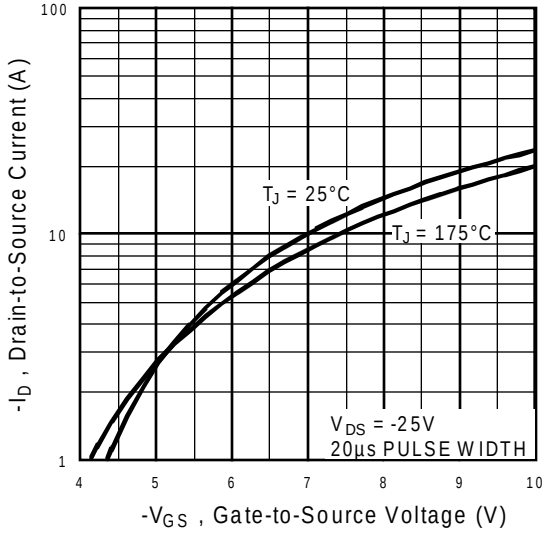


Fig 3. Typical Transfer Characteristics

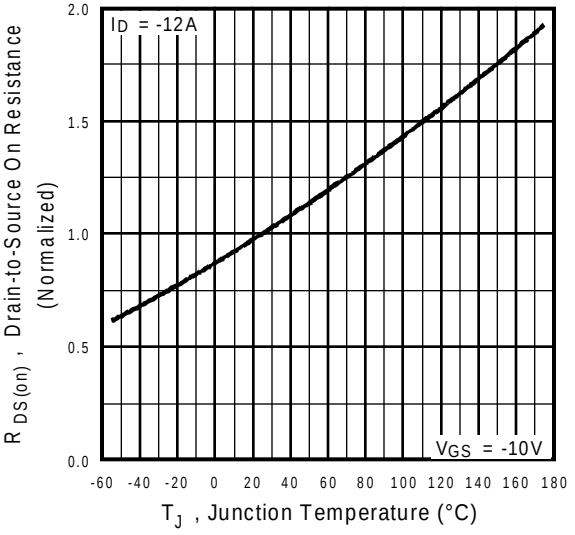


Fig 4. Normalized On-Resistance
Vs. Temperature

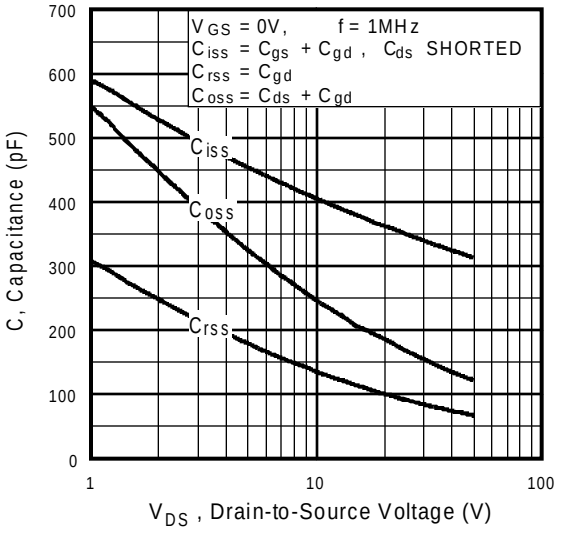


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

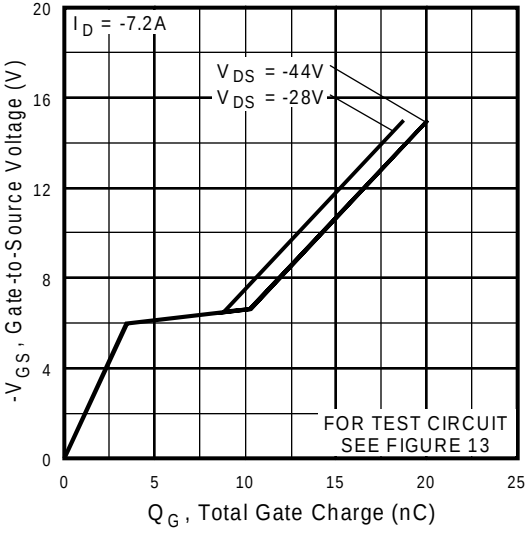


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

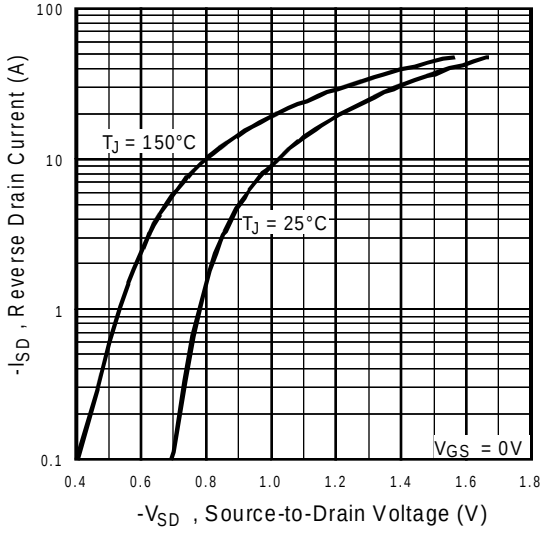


Fig 7. Typical Source-Drain Diode Forward Voltage

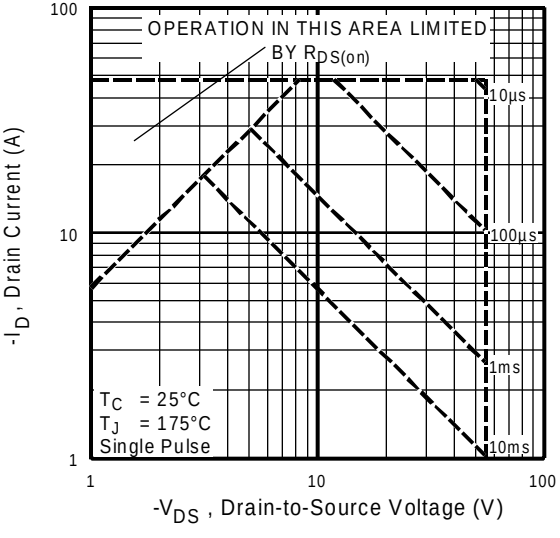


Fig 8. Maximum Safe Operating Area

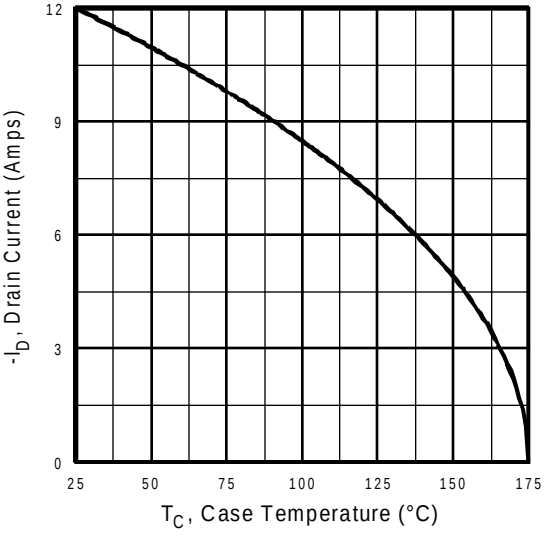


Fig 9. Maximum Drain Current Vs. Case Temperature

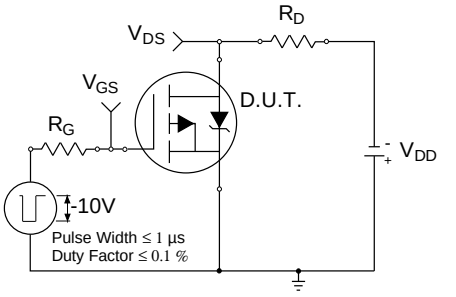


Fig 10a. Switching Time Test Circuit

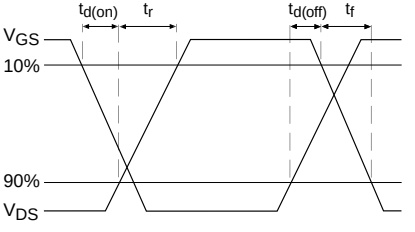


Fig 10b. Switching Time Waveforms

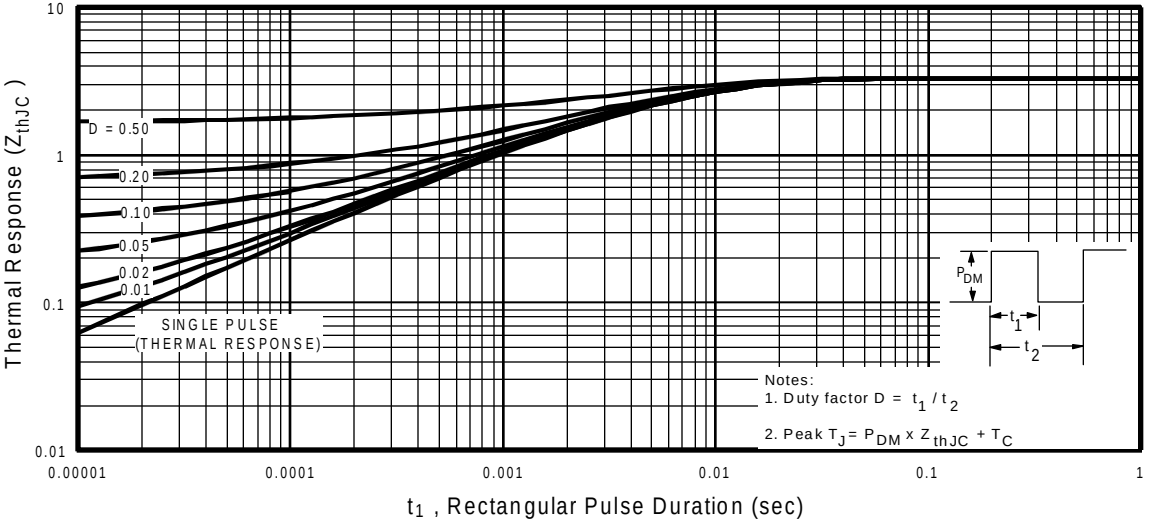


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

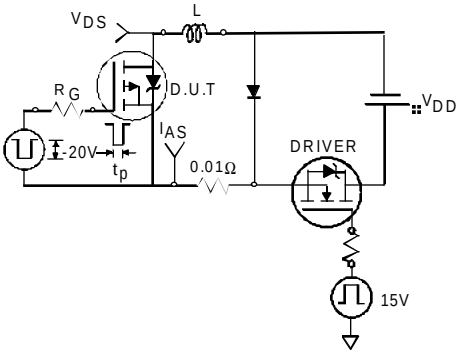


Fig 12a. Unclamped Inductive Test Circuit

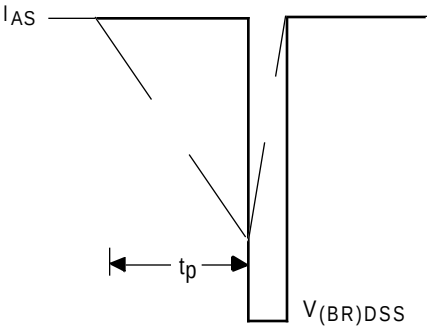


Fig 12b. Unclamped Inductive Waveforms

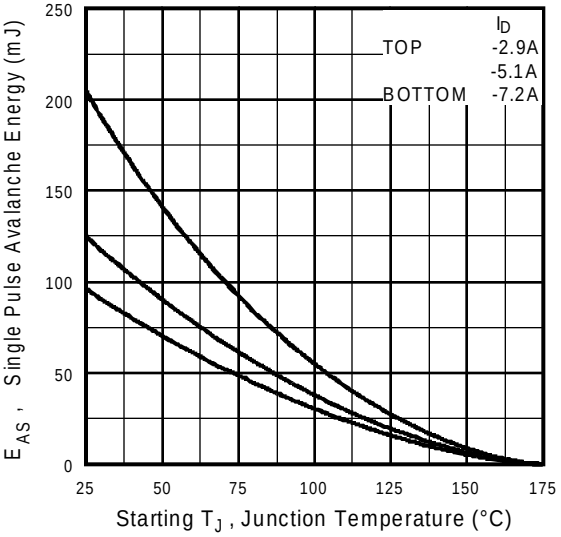


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

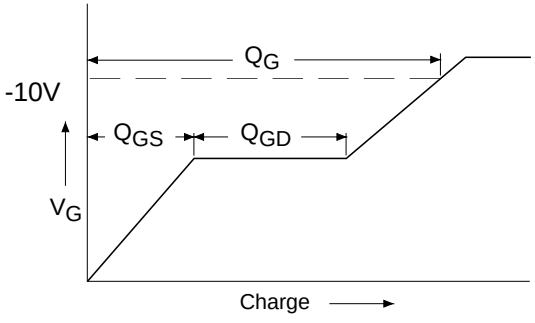


Fig 13a. Basic Gate Charge Waveform

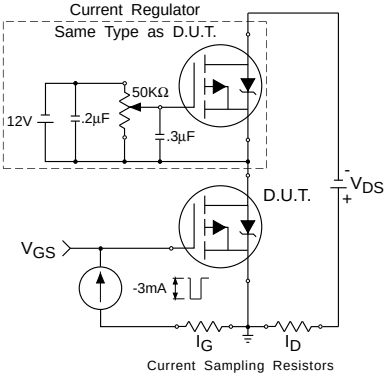
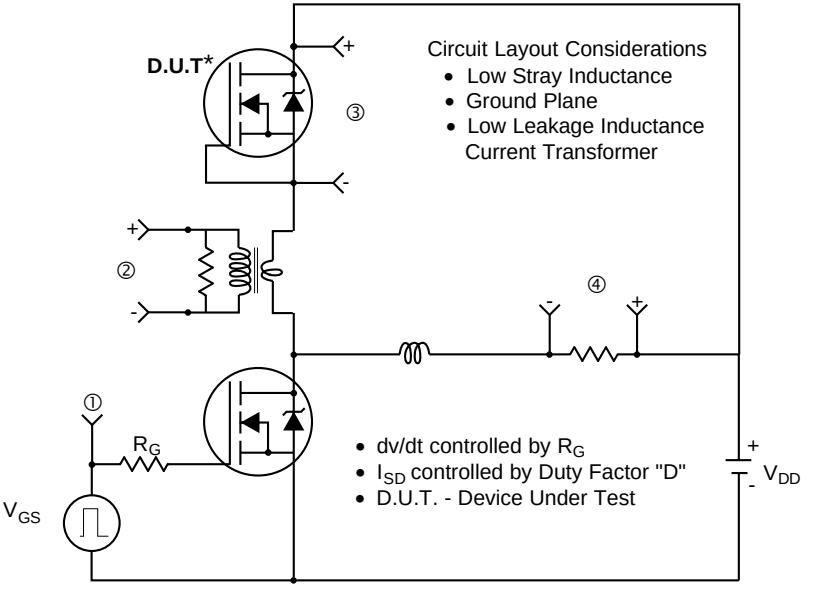
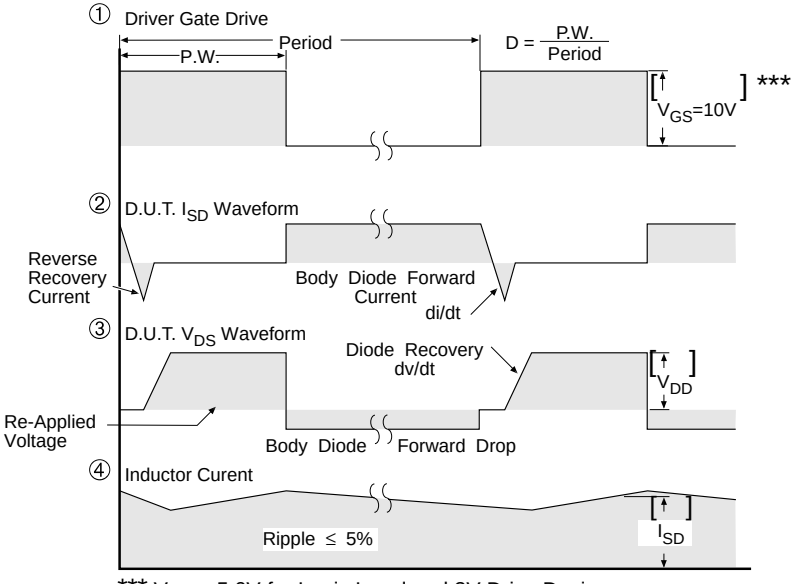


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



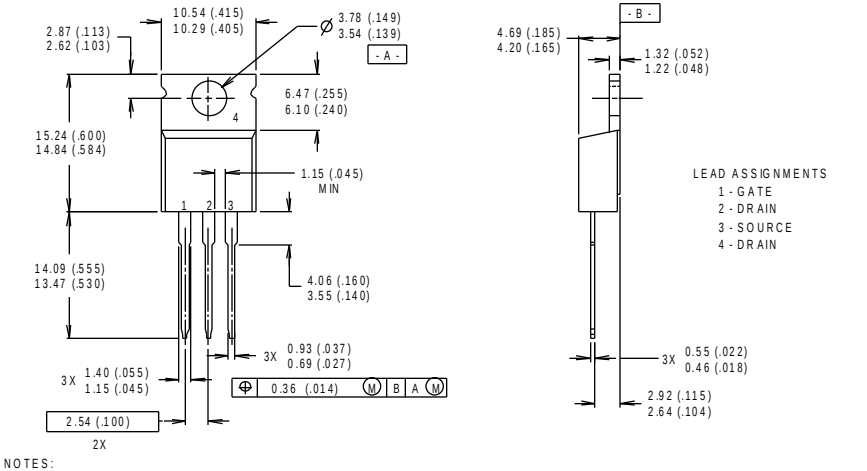
*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 14. For P-Channel HEXFETS

Package Outline

TO-220AB Outline

Dimensions are shown in millimeters (inches)



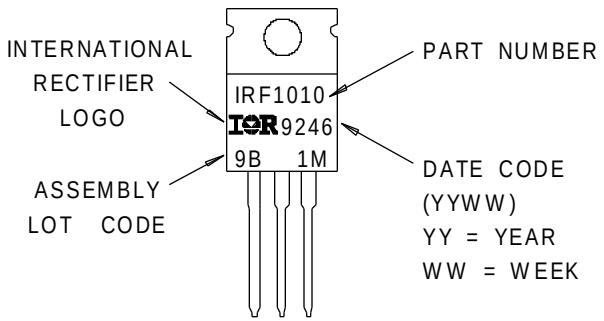
NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH
3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

Part Marking Information

TO-220AB

EXAMPLE : THIS IS AN IRF1010
WITH ASSEMBLY
LOT CODE 9B1M



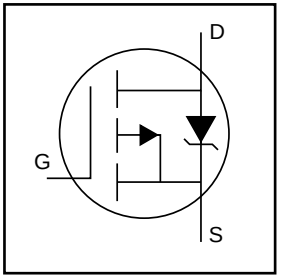
International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 7321 Victoria Park Ave., Suite 201, Markham, Ontario L3R 2Z8, Tel: (905) 475 1897
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ki, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 315 Outram Road, #10-02 Tan Boon Liat Building, Singapore 0316 Tel: 65 221 8371

IRFR/U9024N

HEXFET® Power MOSFET

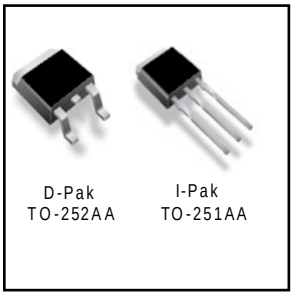
- Ultra Low On-Resistance
- P-Channel
- Surface Mount (IRFR9024N)
- Straight Lead (IRFU9024N)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = -55V

$R_{DS(on)}$ = 0.175Ω

I_D = -11A



Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D-Pak is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.

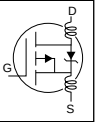
Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ -10V	-11	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ -10V	-8	
I_{DM}	Pulsed Drain Current ①	-44	
P_D @T_C = 25°C	Power Dissipation	38	W
	Linear Derating Factor	0.30	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	62	mJ
I_{AR}	Avalanche Current①	-6.6	A
E_{AR}	Repetitive Avalanche Energy①	3.8	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-10	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

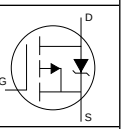
Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	3.3	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)**	——	50	
$R_{\theta JA}$	Junction-to-Ambient	——	110	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-55	—	—	V	V_{GS} = 0V, I_D = -250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.05	—	V/°C	Reference to 25°C, I_D = -1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.175	Ω	V_{GS} = -10V, I_D = -6.6A ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250μA
g_{fs}	Forward Transconductance	2.5	—	—	S	V_{DS} = -25V, I_D = -7.2A⑥
I_{DSS}	Drain-to-Source Leakage Current	—	—	-25	μA	V_{DS} = -55V, V_{GS} = 0V
		—	—	-250		V_{DS} = -44V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	19	nC	I_D = -7.2A
Q_{gs}	Gate-to-Source Charge	—	—	5.1		V_{DS} = -44V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	10		V_{GS} = -10V, See Fig. 6 and 13 ④⑥
$t_{d(on)}$	Turn-On Delay Time	—	13	—	ns	V_{DD} = -28V
t_r	Rise Time	—	55	—		I_D = -7.2A
$t_{d(off)}$	Turn-Off Delay Time	—	23	—		R_G = 24Ω
t_f	Fall Time	—	37	—		R_D = 3.7Ω, See Fig. 10 ④⑥
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact⑤ 
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	350	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	170	—		V_{DS} = -25V
C_{rss}	Reverse Transfer Capacitance	—	92	—		f = 1.0MHz, See Fig. 5⑥

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-11	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-44		
V_{SD}	Diode Forward Voltage	—	—	-1.6	V	T_J = 25°C, I_S = -7.2A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	47	71	ns	T_J = 25°C, I_F = -7.2A
Q_{rr}	Reverse Recovery Charge	—	84	130	nC	di/dt = 100A/μs ④⑥
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 2.8mH R_G = 25Ω, I_{AS} = -6.6A. (See Figure 12)

③ I_{SD} ≤ -6.6A, di/dt ≤ 240A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 150°C

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

⑤This is applied for I-PAK, L_S of D-PAK is measured between lead and center of die contact

⑥ Uses IRF9Z24N data and test conditions.

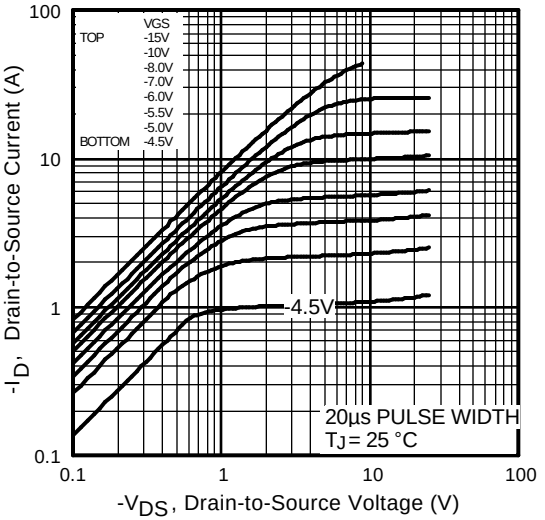


Fig 1. Typical Output Characteristics

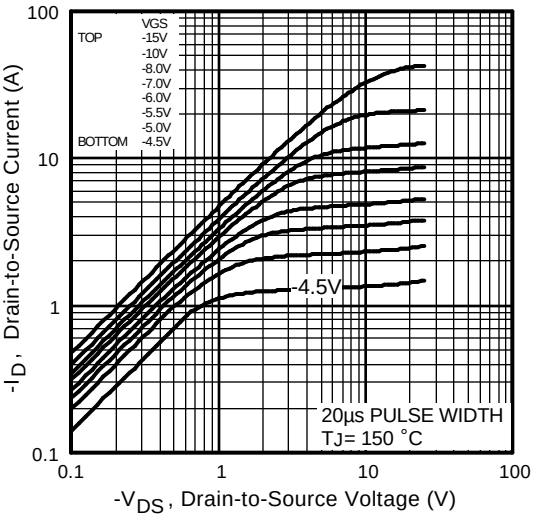


Fig 2. Typical Output Characteristics

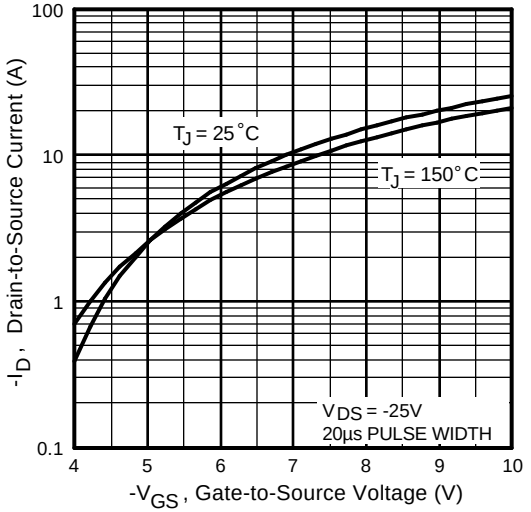


Fig 3. Typical Transfer Characteristics

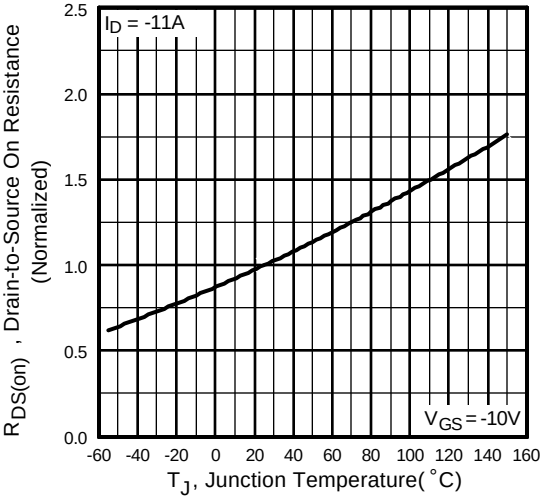


Fig 4. Normalized On-Resistance Vs. Temperature

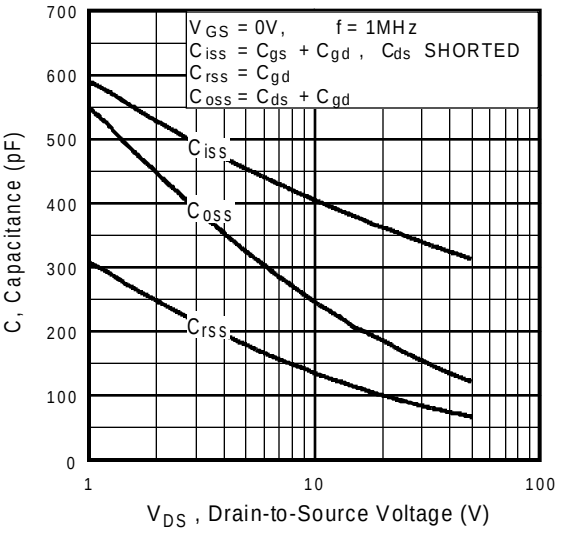


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

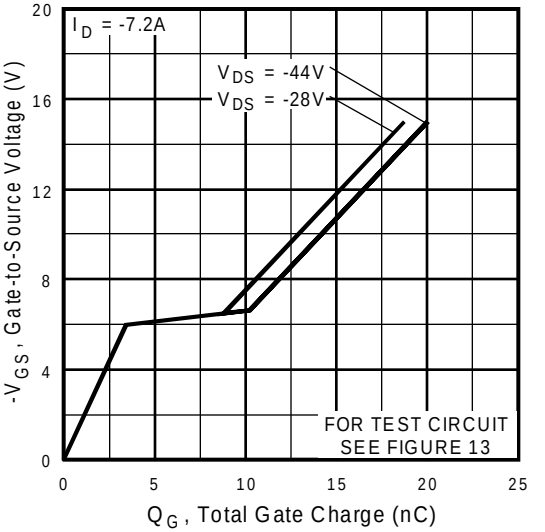


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

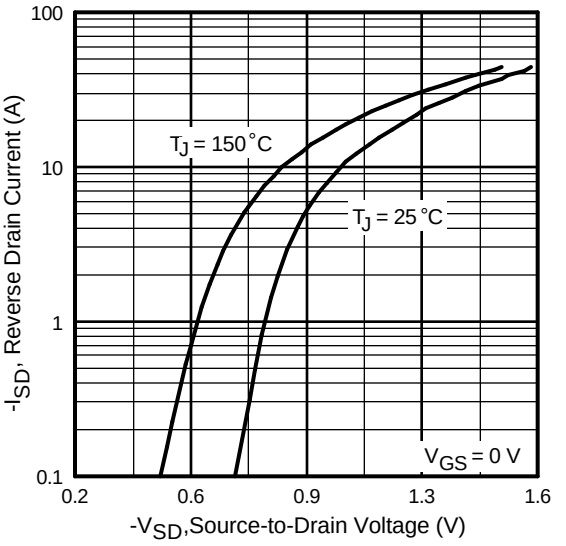


Fig 7. Typical Source-Drain Diode Forward Voltage

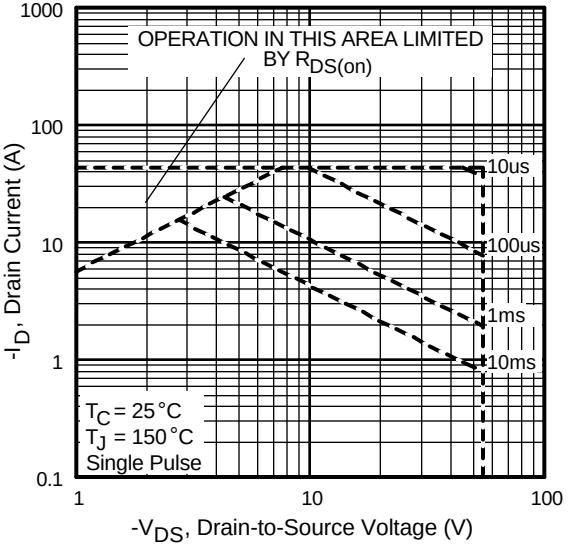


Fig 8. Maximum Safe Operating Area

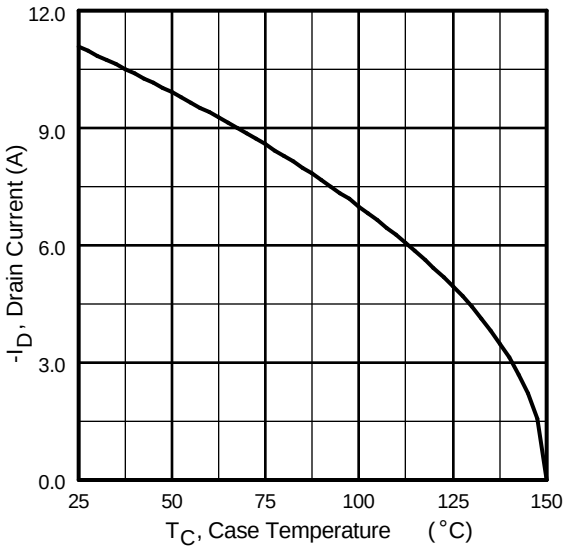


Fig 9. Maximum Drain Current Vs. Case Temperature

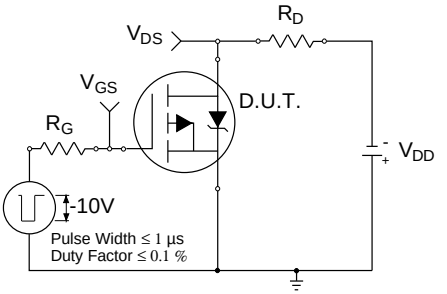


Fig 10a. Switching Time Test Circuit

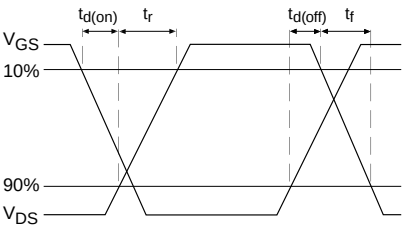


Fig 10b. Switching Time Waveforms

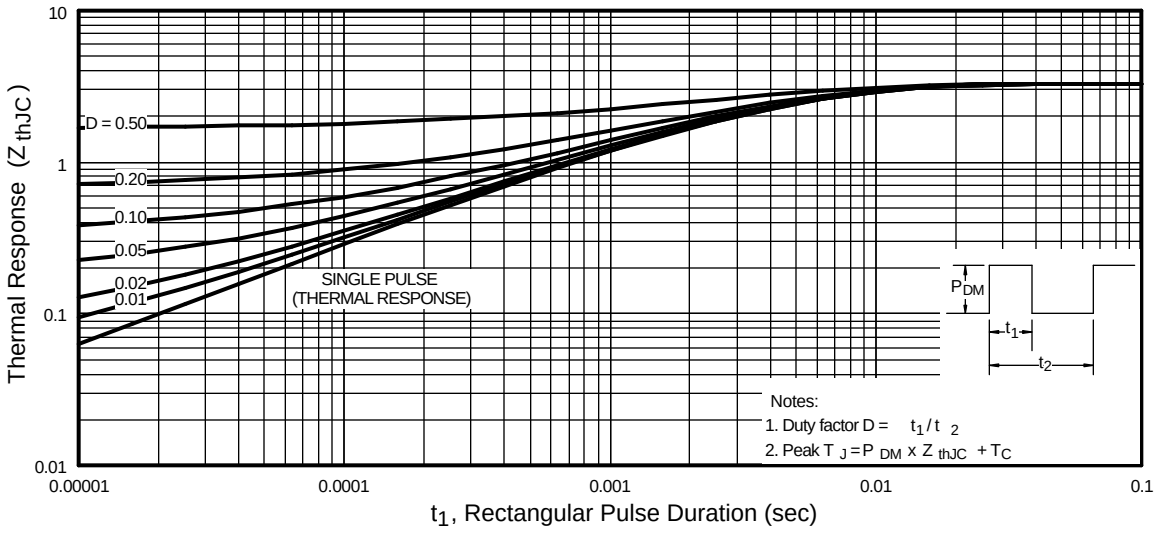


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

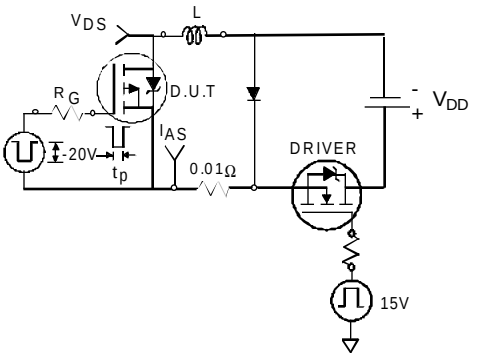


Fig 12a. Unclamped Inductive Test Circuit

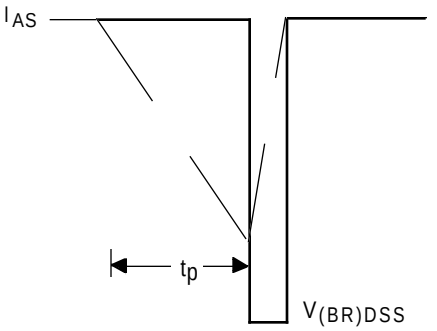


Fig 12b. Unclamped Inductive Waveforms

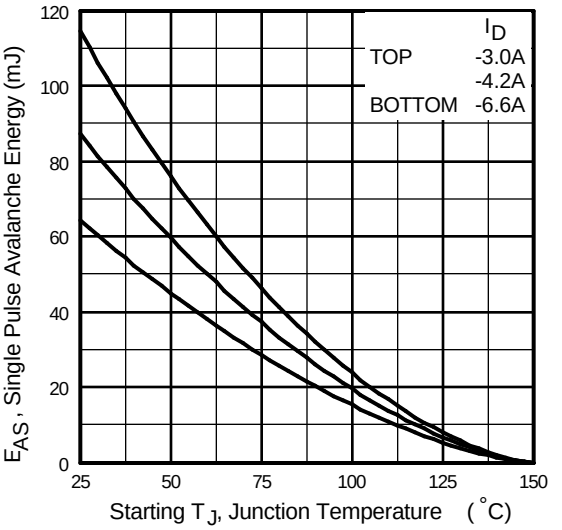


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

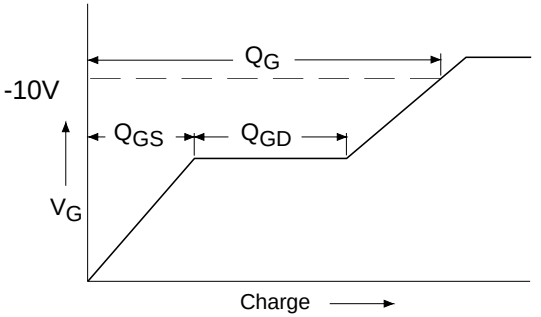


Fig 13a. Basic Gate Charge Waveform

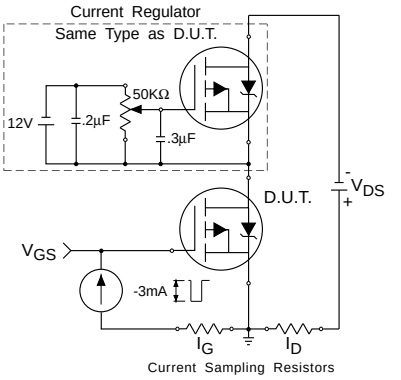
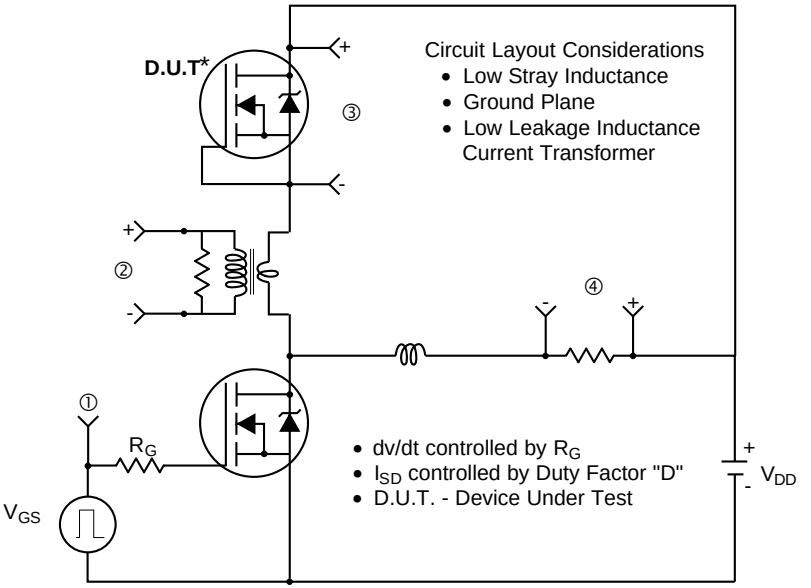
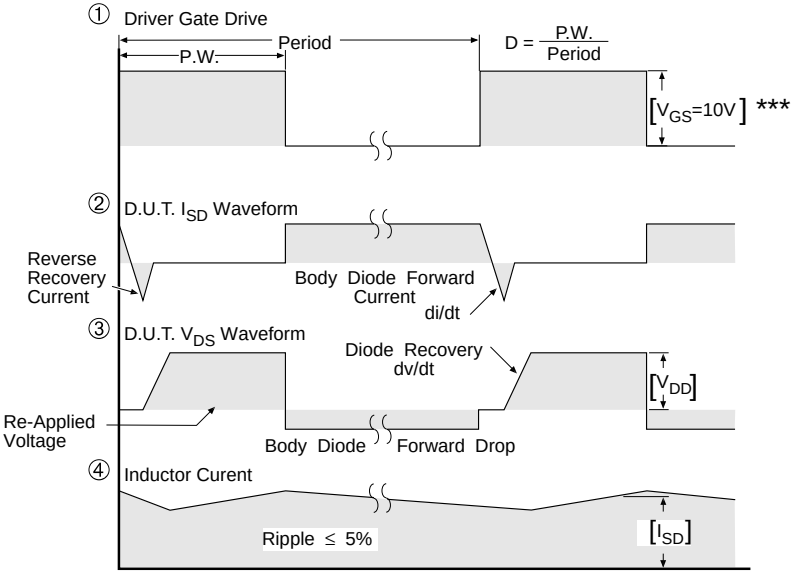


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel

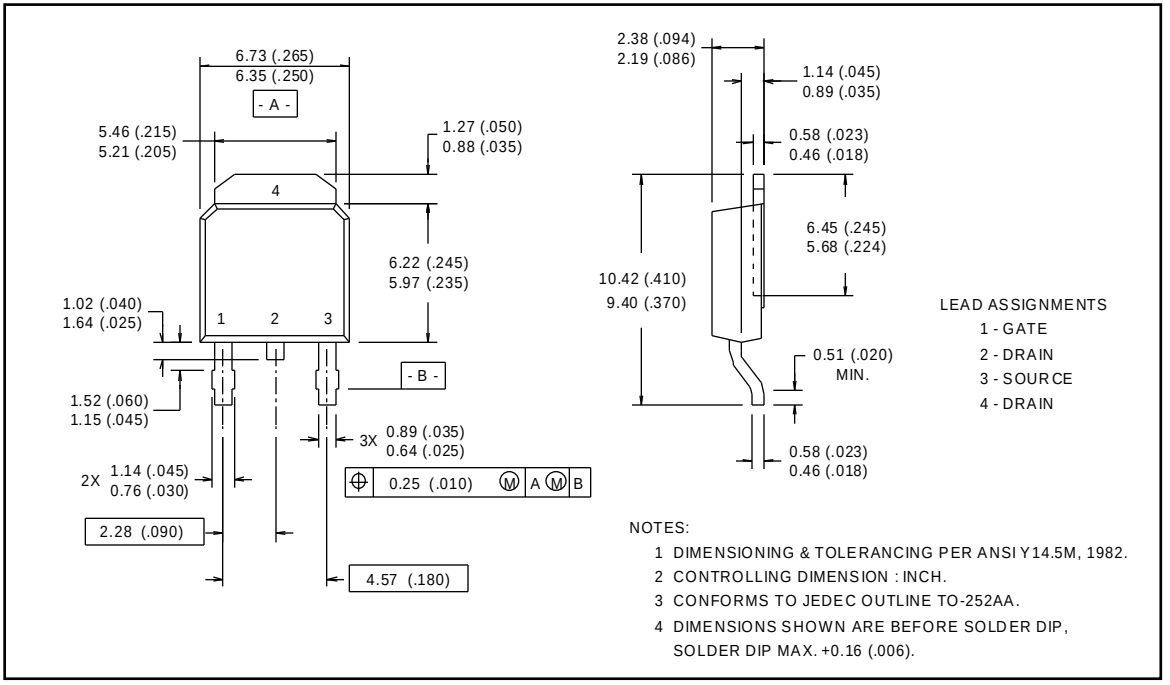


*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 14. For P-Channel HEXFETS

Package Outline

TO-252AA Outline
Dimensions are shown in millimeters (inches)

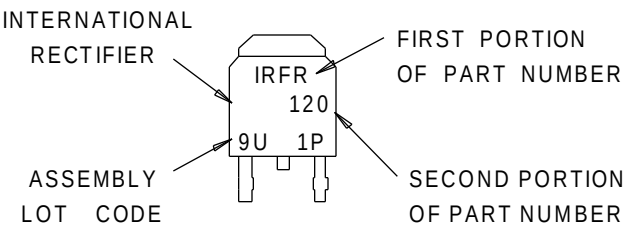


NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

Part Marking Information

TO-252AA (D-Pak)

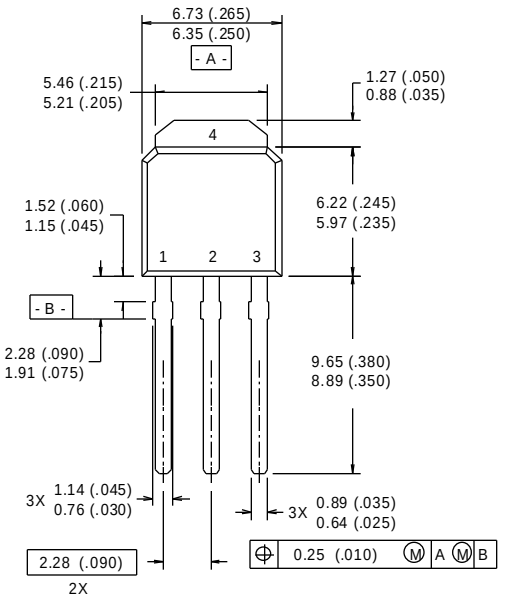
EXAMPLE : THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 9U1P

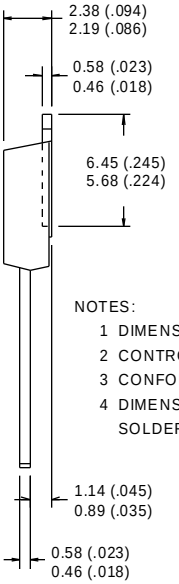


Package Outline

TO-251AA Outline

Dimensions are shown in millimeters (inches)





LEAD ASSIGNMENTS

1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

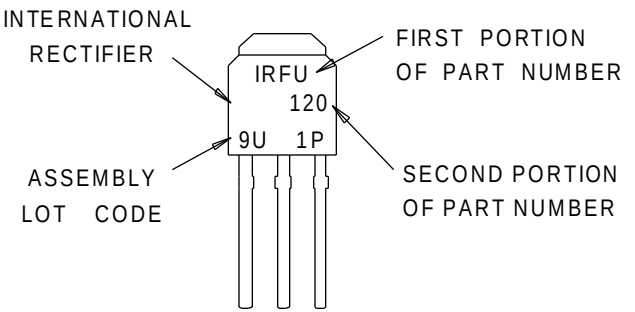
NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

Part Marking Information

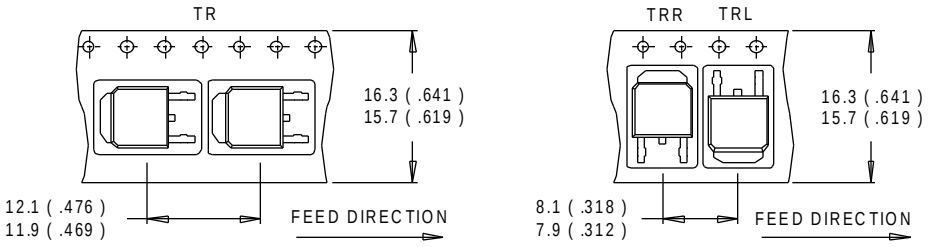
TO-251AA (I-Pak)

EXAMPLE : THIS IS AN IRFU120
WITH ASSEMBLY
LOT CODE 9U1P

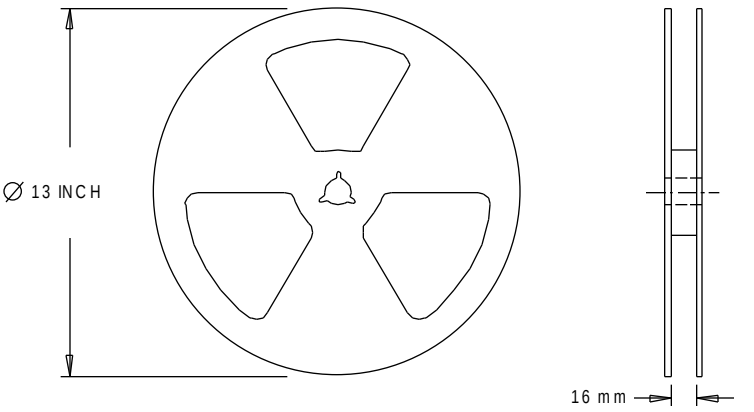


Tape & Reel Information

TO-252AA



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Kingbright

14.2mm (0.56INCH) SINGLE DIGIT NUMERIC DISPLAY

Part Number: SC56-11SURKWA Hyper Red

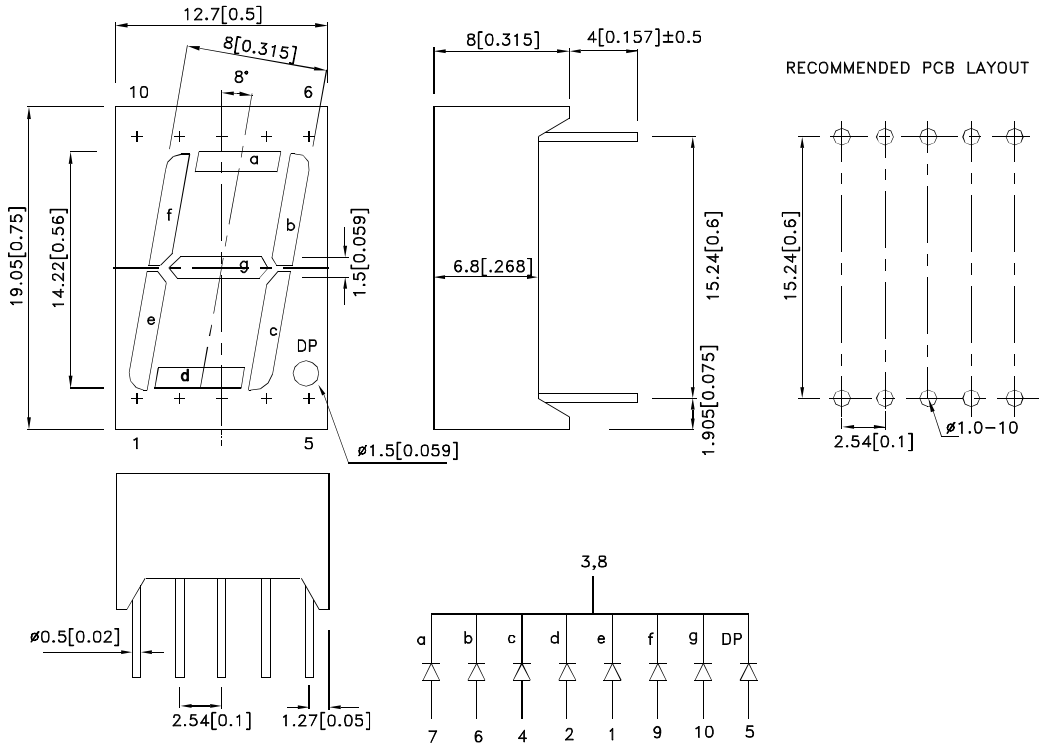
Features

- 0.56 inch digit height.
- Low current operation.
- Excellent character appearance.
- Easy mounting on P.C. boards or sockets.
- Mechanically rugged.
- Standard : gray face, white segment.
- RoHS compliant.

Description

The Hyper Red source color devices are made with Al-GaInP on GaAs substrate Light Emitting Diode.

Package Dimensions& Internal Circuit Diagram



Notes:
1. All dimensions are in millimeters (inches), Tolerance is ±0.25(0.01")unless otherwise noted.
2. The specifications, characteristics and technical data described in the datasheet are subject to change without prior notice.

Selection Guide

Part No.	Dice	Lens Type	Iv (ucd) [1] @ 10mA		Description
			Min.	Typ.	
SC56-11SURKWA	Hyper Red (AlGaInP)	White Diffused	31000	97000	Common Cathode, Rt. Hand Decimal.
			*14000	*27000	

Note:
1. Luminous intensity/ luminous Flux: +/-15%.
* Luminous intensity value is traceable to the CIE127-2007 compliant national standards.

Electrical / Optical Characteristics at TA=25°C

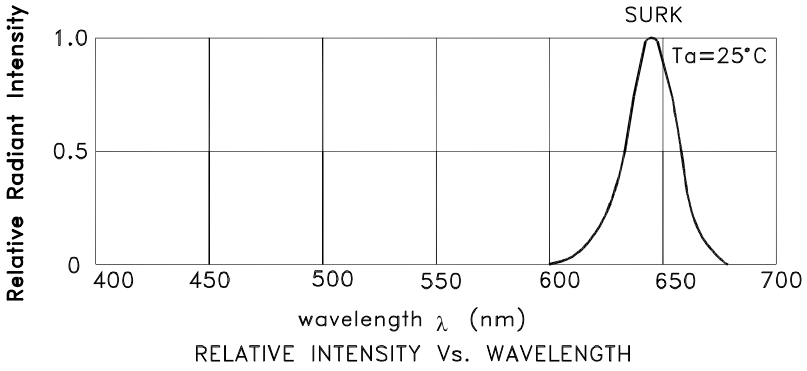
Symbol	Parameter	Device	Typ.		Max.	Units	Test Conditions
λpeak	Peak Wavelength	Hyper Red	650	*645		nm	I_F=20mA
λD [1]	Dominant Wavelength	Hyper Red	630	*630		nm	I_F=20mA
Δλ1/2	Spectral Line Half-width	Hyper Red	28			nm	I_F=20mA
C	Capacitance	Hyper Red	35			pF	V_F=0V;f=1MHz
V_F [2]	Forward Voltage	Hyper Red	1.95		2.5	V	I_F=20mA
I_R	Reverse Current	Hyper Red			10	uA	V_R=5V

Notes:
1.Wavelength: +/-1nm.
2. Forward Voltage: +/-0.1V.
* Wavelength value is traceable to the CIE127-2007 compliant national standards.

Absolute Maximum Ratings at TA=25°C

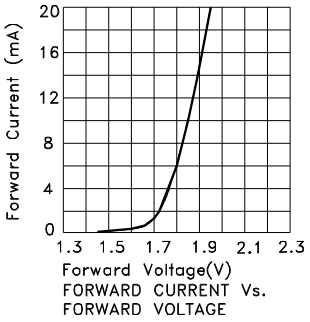
Parameter	Hyper Red	Units
Power dissipation	75	mW
DC Forward Current	30	mA
Peak Forward Current [1]	185	mA
Reverse Voltage	5	V
Operating / Storage Temperature	-40°C To +85°C	
Lead Solder Temperature[2]	260°C For 3-5 Seconds	

Notes:
1. 1/10 Duty Cycle, 0.1ms Pulse Width.
2. 2mm below package base.

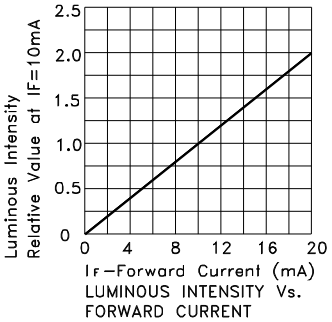


RELATIVE INTENSITY Vs. WAVELENGTH

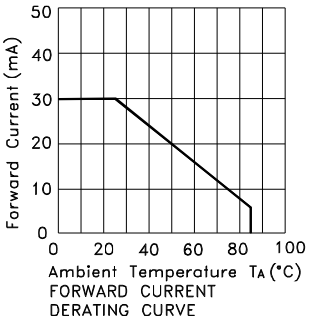
Hyper Red **SC56-11SURKWA**



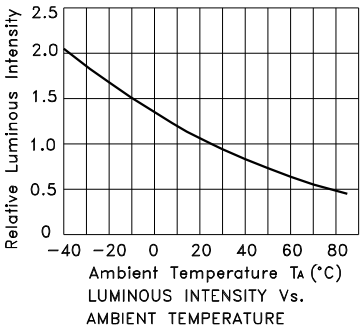
FORWARD CURRENT Vs.
FORWARD VOLTAGE



LUMINOUS INTENSITY Vs.
FORWARD CURRENT

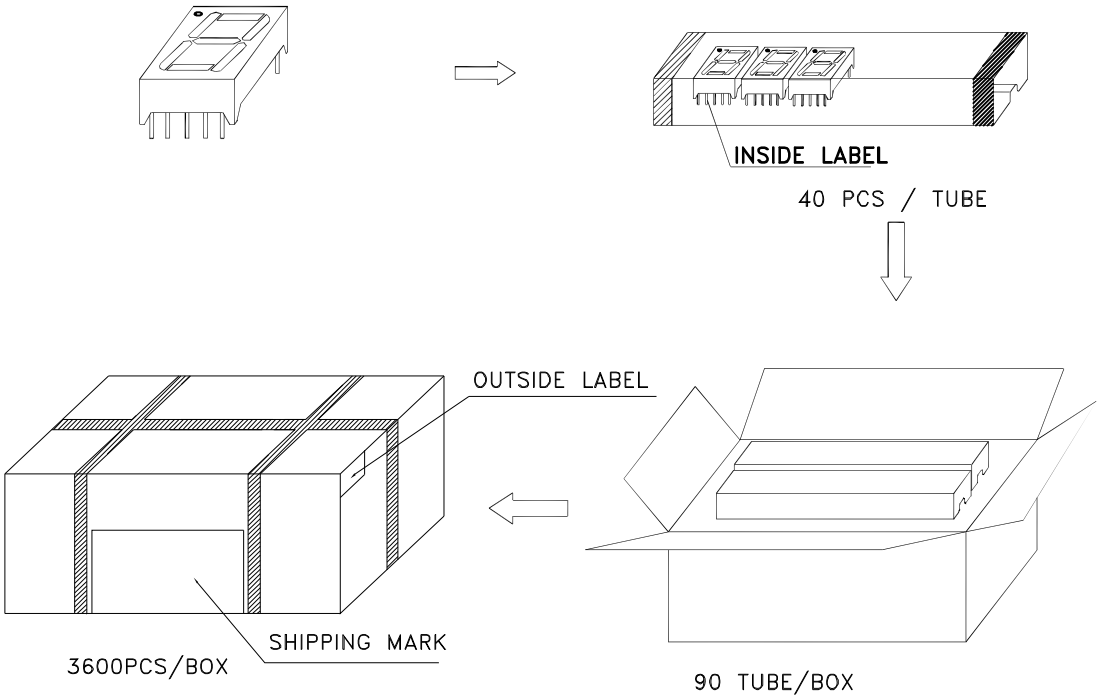


FORWARD CURRENT
DERATING CURVE

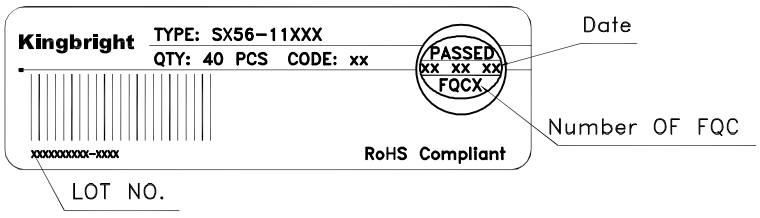


LUMINOUS INTENSITY Vs.
AMBIENT TEMPERATURE

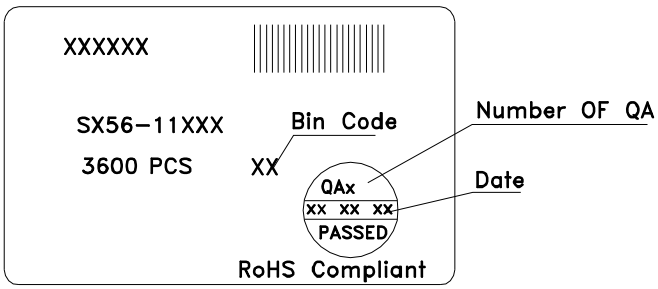
PACKING & LABEL SPECIFICATIONS **SC56-11SURKWA**



Inside Label On IC-TUBE



Outside Label On Box

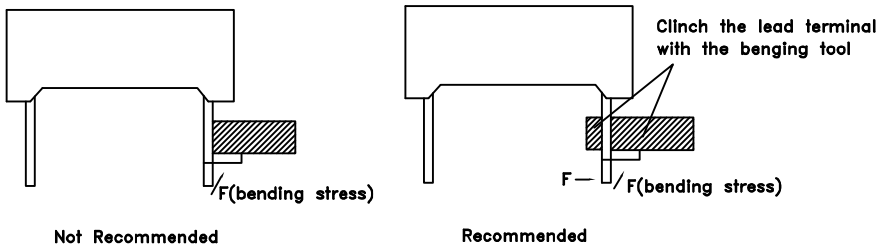


THROUGH HOLE DISPLAY MOUNTING METHOD

Lead Forming

Do not bend the component leads by hand without proper tools.

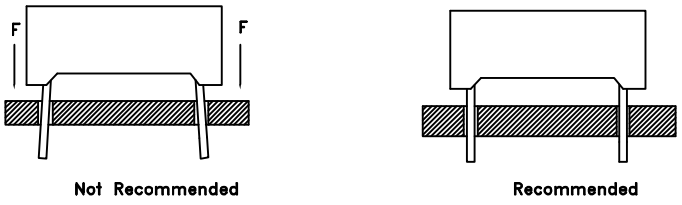
The leads should be bent by clinching the upper part of the lead firmly such that the bending force is not exerted on the plastic body.



Installation

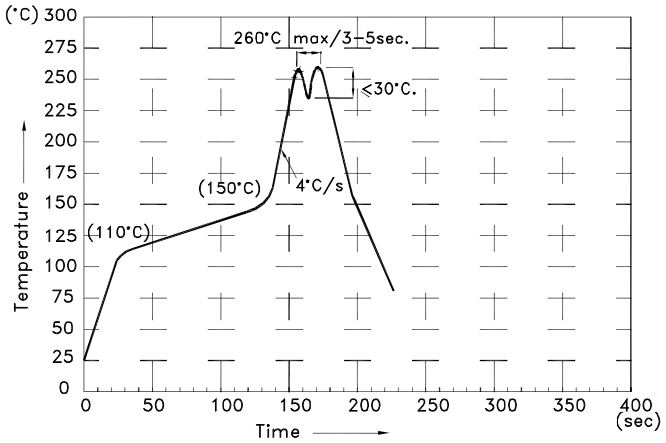
1.The installation process should not apply stress to the lead terminals.

2.When inserting for assembly, ensure the terminal pitch matches the substrate board's hole pitch to prevent spreading or pinching the lead terminals.



DISPLAY SOLDERING CONDITIONS

Wave Soldering Profile For Lead-free Through-hole LED.



NOTES:

1.Recommend the wave temperature 245°C~260°C.The maximum soldering temperature should be less than 260°C.

2.Do not apply stress on epoxy resins when temperature is over 85°C.

3.The soldering profile apply to the lead free soldering (Sn/Cu/Ag alloy).

4.During wave soldering , the PCB top-surface temperature should be kept below 105°C

5.No more than once.

Soldering General Notes:

a. Through-hole displays are incompatible with reflow soldering.

b. If components will undergo multiple soldering processes, or other processes where the components may be subjected to intense heat, please check with Kingbright for compatibility.

CLEANING

1.Mild "no-clean" fluxes are recommended for use in soldering.

2. If cleaning is required, Kingbright recommends to wash components with water only. Do not use harsh organic solvents for cleaning, because they may damage the plastic parts .And the devices should not be washed for more than one minute.

CIRCUIT DESIGN NOTES

1.Protective current-limiting resistors may be necessary to operate the Displays.

2.LEDs mounted in parallel should each be placed in series with its own current-limiting resistor.

